PATENT **01AB077/ALBRP228US**

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5-25-06
Date:

Himanshu S. Amin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Mark Flood, *et al.*

Serial No: 09/862,941

Filing Date: May 22, 2001

Examiner: Kyung H. Shin

Art Unit: 2143

Title: APPARATUS FOR MULTI-CHASSIS CONFIGURABLE TIME SYNCHRONIZATION

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REPLY BRIEF

Dear Sir:

Appellants' representative submits this Reply Brief in response to the Examiner's Answer dated April 7, 2006. A credit card payment form is filed concurrently herewith, wherein the credit card payment form is believed to cover all fees due regarding this document. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP228US].

REMARKS

Claims 1-52 are currently pending and are presently under consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein. In particular, the following comments address deficiencies contended in the Examiner's Answer to applicants' Appeal Brief.

I. Regarding the Rejection of Claims 1-7, 13-28, 30-34, 38-46 and 48-52 Under 35 U.S.C. §102(e)

The Examiner incorrectly maintains the rejection of claims 1-7, 13-28, 30-34, 38-46 and 48-52 under 35 U.S.C. §102(e) as being unpatentable over Voth (US 6,199,169). It is respectfully submitted that this rejection should be reversed for at least the following reasons. Voth does not teach or suggest all features of the subject claims.

> A **single** prior art reference anticipates a patent claim only if it expressly or inherently describes ***each and every limitation set forth in the patent claim.*** *Trintec Industries, Inc., v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 U.S.P.Q.2D 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). ***The identical invention must be shown in as complete detail as is contained in the ... claim.*** *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Appellants' claimed subject matter relates generally to industrial control systems (*see, e.g.*, control system 50, FIG. 2) with a time synchronization apparatus (*see, e.g.*, S/L 82, FIG. 2) for synchronizing operation of a first controller (*see, e.g.*, controller 56, FIG. 2) with that of a second controller (*see, e.g.*, controller 54, FIG. 2). More specifically, the time synchronization apparatus can be interfaced to a host processor (*see, e.g.*, PLC 72, FIG. 2) *via* a processor interface such as a bus or common backplane (*see, e.g.*, page 10, ll. 17-18). The first controller can communicate synchronization information to the second controller *via* a synchronization network (*see, e.g.*, network 84, FIG. 2) and can communicate control information, data, configuration information to the second controller *via* a communication network (*see, e.g.*, page 10, ll. 22-26; network 80, FIG. 2). In particular, independent claim 1 (and similarly independent

claims 38, 39 and 52) recites, "*A **time synchronization apparatus*** for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising: a ***processor interface*** for interfacing ***the synchronization apparatus*** with a ***host processor***; a ***transmitter*** adapted to *transmit synchronization information **and data*** to a ***network in the control system; a receiver***... and ***a timing system with a clock***". Voth does not teach or suggest these novel features.

Rather, Voth relates to a method of time synchronization in a single system image (SSI) cluster. (*See* col. 2, ll. 54-57). The system includes a master node and a plurality of slave nodes, interconnected *via* a computer network (*see* FIG. 1; col. 4, ll. 7-17), and employs native operating system commands to affect time synchronization between the nodes (*see* col. 4, ll. 64-67; FIG. 4; *e.g.*, the SYNC and INFO commands represent the operating system commands). Hence, Voth discloses a system that can synchronize operation of a first node with that of a second node, however, Voth does not teach or suggest the ***time synchronization apparatus*** of the subject claims. That is, Voth does not disclose sufficient structure or structural interrelationships to anticipate the claimed apparatus.

In particular, the subject claims expressly recite a time synchronization apparatus comprising: 1) a processor interface... 2) a transmitter... 3) a receiver... and 4) a timing system. As well, many of these features are expressly indicated to interface other claimed structure. Since, at a holistic level, Voth can perform a similar function, *i.e.*, time synchronization, albeit in an entirely different manner and with different disclosed structure, the Examiner presumes the inventions are identical without ever considering the claims as a whole. For example, the Examiner has not identified any consistent feature of Voth that anticipates the synchronization apparatus. The Office Action (dated October 6, 2004) merely indicated various structures in Voth that when considered piecemeal can perform similar *function* as some analogous features of the synchronization apparatus, but without the claimed *structure*. (*See* Office Action, pages 2-3). In the Final Office Action (dated June 30, 2005), the Examiner inappropriately indicated that the synchronization apparatus was the entire system of Voth, (*i.e.*, system 100 of FIG. 1), which again failed to teach or suggest the necessary structural interrelationships recited in the claims. (*See* Final Office Action, page 2). Finally, in the Examiner's Answer (dated April 7, 2006, hereinafter "EA") it is indicated at pages 20-21 that the synchronization apparatus is actually a

single processor disclosed in Voth, *e.g.*, "one processor dedicated...to the time synchronization process[es]" that substantially provides "the time synchronization service."

The Examiner relies upon a number of statements not substantiated by the reference. For example, the Examiner hypothesizes that Voth teaches dedicated processors and dedicated network adapters in the sense that one processor and one network adapter performs only time synchronization functions, while the other processor and network adapter performs only other computer processes. (*See* EA, page 20). Voth does not teach these aspects and the Examiner provides no citations. Apart from these unsubstantiated, hypothetical features of the reference, even if Voth did disclose dedicated processors (and dedicated network adapters), the "processor dedicated to time synchronization processes" still does not constitute the time synchronization apparatus of the subject claims, even if the processor can provide a "time synchronization service." In fact, the processor in Voth teaches none of the indicated structure, *i.e.*, the processor does not comprise 1) a processor interface for interfacing the synchronization apparatus with a host processor; 2) a transmitter adapted to transmit synchronization information and data to a network in the control system 3) a receiver... and 4) a timing system with a clock. Voth may disclose structure that, in a vacuum and when considered piecemeal performs similar function, but the resident structure is not present. Moreover, these features (if any) are not contained in the processor itself, so the processor cannot anticipate the claimed apparatus. Once more, the Examiner's analysis rests entirely on an argument that some time synchronization is occurring, irrespective of the explicit limitations of the claims. Pointedly, appellants' are not attempting to claim time synchronization, but rather ***a time synchronization apparatus***. All of the Examiner's attempts to isolate particular features of Voth to read on the claimed subject matter have failed, largely because Voth is materially deficient to disclose the time synchronization apparatus recited in the subject claims.

Appellants' representative does not dispute that Voth can synchronize one node with respect to a second node, however, such a feature is not sufficient to anticipate appellants' claims. For example, a node in a single system image (SSI) cluster is neither a controller in a control system nor the synchronization apparatus of the subject claims, yet the Examiner's analysis required it to represent both, simultaneously if a node is considered to be the synchronization apparatus. Similarly, a processor of one of the nodes is not the synchronization apparatus either, for substantially the same reasons: the claimed structure does not exist no

matter how the features disclosed in Voth are dissected and/or arranged. For example, the processor 202 is not comprising the time clock 212 (*see* FIG. 2), so the processor does not read on the claimed apparatus. Likewise, the entire system disclosed in Voth is not the synchronization apparatus either since, *inter alia*, the analysis requires the network 104 to represent both the processor interface and the network in the control system, simultaneously. In all cases, the Examiner's analysis is forced to substitute certain components disclosed in Voth in ways that are mutually exclusive and/or inconsistent with the claimed features in order to arrive at the erroneous conclusion that the claims are anticipated. Appellants' representative respectfully submits that Voth was employed as a reference simply because of the similarity in a single particular *function*: time synchronization. That alone, is not sufficient to anticipate the subject claims.

In addition, at page 5 of the EA, it is incorrectly argued that Voth discloses the time synchronization apparatus of claims 4 and 15, wherein the fixed period is about 50μs. To the contrary, Voth teaches a period of 4 seconds, which is materially distinct from about 50μs. (*See* col. 4, ll. 43-54; FIG. 3, wherein the time axis shows 4 seconds between the repeating cycle 306 and 306'), which is about five orders of magnitude greater than 50μs. The Examiner does not argue 4 seconds is similar to about 50μs, rather, the Examiner cites a passage from the specification portion of the appellants' disclosure that recites "the synchronization component can transmit (broadcast) a frame every 50μs or some other fixed time period." In essence, the Examiner rejects these claims because supporting passages in the specification would allow broader claims, *e.g.*, 50μs *or some other fixed time period.* It is the claims that define the metes and bounds of an invention, not the specification. The claims expressly recite about 50μs. Some other fixed time period such as 4 seconds does not read upon these claims simply because the specification contemplates other time periods. The Examiner impermissibly employs similar analysis to reject claims 6 and 17 as well.

In view of at least the foregoing, it is readily apparent that Voth does not teach or suggest each and every aspect of the subject claims. Accordingly, this rejection of independent claims 1, 38, 39 and 52, as well as all associated dependent claims, should be reversed.

II. **Regarding the Rejection of Claims 8-12 Under 35 U.S.C. §103(a)**

The Examiner incorrectly maintains the rejection of claims 8-12 under U.S.C. §103(a) as being unpatentable over Voth (US 6,199,169) in view of Ramussen, et al. (US 6,449,732). Reversal of this rejection is respectfully requested because Voth and Ramussen, *et al.*, either alone or in combination, fail to teach or suggest the appellants' claimed subject matter. In addition, Voth is directed toward non-analogous art and is therefore not reasonably pertinent to be relied upon as a basis for rejection.

Claims 8-12 depend directly or indirectly upon independent claim 1. As noted *supra*, Voth does not teach or suggest the claimed subject matter. Ramussen, *et al.* fails to make up for the aforementioned deficiencies of Voth. Therefore, the combination of Ramussen, *et al.* with Voth does not teach or suggest every feature of the instant claims and this rejection should be reversed. Moreover, Voth is non-analogous art. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 144, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). See also *In Re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Voth relates to a method of synchronization, however, this method employs software rather than hardware and is very limited because it works in a Single System Image (SSI) computer cluster (*see* col. 4, ll. 35-38) that requires a very high speed network (*see* col. 4, ll. 19-22), whereas the claimed subject matter recites a synchronization apparatus/circuitry for use with industrial controllers in a distributed control system network. For example, in Voth, the maximum round-trip time of a SYNC message sent from the master to the slave and back to the master is assumed to be no more than 1 microsecond (*i.e.*, 1μs). (*See* col. 8, ll. 44-56). While this round-trip time of 1μs is exemplary, and other values are contemplated (up to 5μs; *see* col. 8, ll. 64-66), the precision of the synchronization algorithm is proportionate to the speed of the network. (*See* col. 8, ll. 57-58).

In order to affect synchronization, the round-trip time for a SYNC message must be less than half of a clock tick, where a clock tick is taught to be 10μs. (*See* col. 8, ll. 60-66). The synchronization algorithm effectively treats the propagation time (*i.e.*, latency) between the nodes as zero when synchronizing, which is why the round-trip time must be extremely short or about 1μs, and also why this method applies only to SSI computer clusters or similar systems

with very high speed networks of a particular topology. Put another way, the synchronization method disclosed in Voth fails and is therefore useless if the round-trip time for messages transmitted between nodes is more than about 5μs. This limitation provides only a very narrow range of use and requires very specific architecture. The reference's synchronization method will not work in conventional networks in a control system or with controllers that communicate with other controllers outside the time zone or outside the first control chassis. For example, the latency between the controllers can be on the order of 50μs (producing a 100μs round-trip time), which is about 20 times too imprecise to affect synchronization using the method disclosed in Voth. Moreover, Voth cannot function in topologies other than a star topology wherein all slave nodes are directly connected to the master node, whereas conventional networks in a control system assume many topologies, such as a daisy-chain and ring topologies. In various other topologies, the round-trip time to communicate from the master to all slave nodes and back can be on the order of 1200 milliseconds, which is about 240,000 times too imprecise to affect synchronization by employing the method of Voth. Moreover, Voth relies upon inherent operating system calls such as the UNIX SYNC message, whereas typical controllers in a control system are not installed with full-service operating systems intended for commercial use. As such, Voth cannot function within conventional industrial control system network environments, and is therefore not "reasonably pertinent to the particular problem with which the inventor was concerned."

At page 23 of the EA, the Examiner submits Voth is analogous art, once more relying solely on the observation that Voth discloses a time synchronization system and the "applicant's invention discloses a time synchronization apparatus." Therefore Voth is analogous art. This suggestion is tantamount to the notion that Voth, because it discloses one way of synchronizing nodes, therefore anticipates all forms of time synchronization, regardless of missing structure and even in systems in which Voth cannot function. This assertion is false. The novelty of Voth is not that it can synchronize nodes, but rather the manner in which the synchronization is achieved (*i.e.*, treating latency between nodes as zero as long as the round-trip time is below a certain tolerance of one-half a clock cycle). The Examiner tacitly ignores that Voth is directed to time synchronization of nodes *in a SSI system*, whereas the subject claims are directed to a time synchronization apparatus for synchronization operation *in a control system*. Voth is rendered utterly inoperable outside of very narrow constraints and, thus, does not address the particular

problem with which appellant was concerned. Accordingly, Voth is not reasonably pertinent and this rejection should be reversed.

III. **Regarding the Rejection of Claims 29, 35, 36, 37 and 47 Under 35 U.S.C. §103(a)**

The Examiner incorrectly maintains the rejection of claims 29, 35, 36, 37 and 47 under U.S.C. §103(a) as being unpatentable over Voth (US 6,199,169) in view of Kuribayashi, *et al.* (US 6,775,246). Reversal of the rejection is respectfully requested for at least the following reasons. Voth and Kuribayashi, *et al.*, alone or in combination, do not teach or suggest the appellants' claimed subject matter. Voth relates to non-analogous art and cannot be relied upon as a basis for rejection.

Claims 29 and 35-37 depend directly or indirectly upon independent claim 1 while claim 47 depends directly or indirectly upon independent claim 39. As noted *supra*, Voth fails to teach or suggest appellants' claimed subject matter as recited in the subject claims. Kuribayashi, *et al.* fails to make up for the aforementioned deficiencies of Voth with respect to independent claims from which claims 29, 35-37 and 47 depend, respectively. Moreover, as submitted *supra* with respect to the rejection of claims 8-12, Voth is non-analogous art, and as such cannot be used as a basis for rejection. Accordingly, this rejection should be reversed.

In addition, dependent claim 35 recites, the time synchronization apparatus of claim 1, being configured as an intermediate node in a ***daisy-chain topology***, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. Neither Voth nor Kuribayashi, *et al.* teach or suggest a daisy-chain topology. The examiner alleges that Kuribayashi, *et al.* teaches a daisy-chain topology, yet neither the indicated portions nor anywhere else does the reference teach this aspect. Moreover, the method disclosed in Voth relies on direct and nearly instantaneous communication between the nodes in order to affect time synchronization because the method treats the round-trip time of communication between the nodes as zero. Therefore, even if Kuribayashi, *et al.* did teach a daisy-chain topology, the combination of a daisy-chain topology from Kuribayashi, *et al.* would render the time synchronization method disclosed in Voth inoperable because at least one clock cycle would be required to assert an instruction to forward the SYNC message to another node (and more clock cycles for each node connected along the daisy-chain), thereby guaranteeing that all

round-trip times will exceed the maximum allowable value (*i.e.*, one-half of a clock cycle) and be rejected, terminating the method without any synchronization occurring. (*See* col. 6, ll. 50-55).

IV. Conclusion

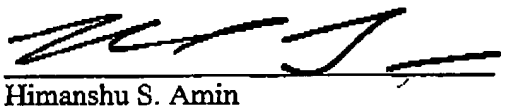
The subject application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN, TUROCY & CALVIN, LLP



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